MEASUREMENT BASED NONLINEAR ELECTROTHERMAL MODELING OF GaAs FET WITH DYNAMICAL TRAPPING EFFECTS

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Abstract — This paper presents MESFET measurement methods based on pulsed measurements that separate trapping and thermal effects. Derived from these measurements, a model of trapping effect is determined, as well as a thermal model. The proposed nonlinear model is validated from DC to RF frequencies, it handles dynamical dispersive effects, it doesn't depend on the hot bias point.

I - INTRODUCTION

GaAs FETs are known to be prone to trapping effects which arise from the capture and emission of electrons injected in the semi-insulated substrate by deep level traps. The trapping process results in strong dependencies of I(V) characteristics in drain-source voltage slow dynamics. This makes the modeling process difficult to be carried out as the RF I(V) characteristics strongly differ from DC ones. This drawback can be eliminated by using pulsed measurements [1], [2], [3], [4] which allow to derive a set of output characteristics for a particular quiescent bias point, as long as the pulse duration is much inferior to the emission process time constant.

However, changing the bias levels requires to remodel the device for this new quiescent state. Obtaining a unique nonlinear model independent from the quiescent bias levels is thus of prime importance. Moreover this model must be able to take into account the thermal behavior of the device. Some authors [5] have addressed this problem by adding the quiescent voltages as new parameters of the model thus taking into account traps and thermal effects in a simple expression.

Our approach is different : trapping and thermal effects are separated in the measurement process and in the model. Moreover, the proposed model takes into account the trap and thermal dynamical behavior which can be important for prediction of slowly-varying envelope modulation of RF signals.

Firstly, we present the effects of traps on pulsed I(V) measurements, with a particular care to avoid thermal effects. Secondly, we propose a method to obtain the model parameters of trapping effects from these measurements. Thermal characterization and modeling is presented. Finally, we demonstrate a general nonlinear model of MESFETs for RF circuit C.A.D. software taking into account the trap and thermal dynamic behavior.

II - PULSED MEASUREMENTS OF TRAPPING EFFECTS

A- Isothermal I(V) characteristics

Pulsed measurement techniques allow to perform nonlinear isothermal characterization of devices. With a pulse measurement set-up, the device is driven and measured during very short pulses (about 300 ns) performed around a fixed bias point. The pulse duration is much shorter than the thermal time constant and the period is large enough to ensure that the device temperature is controlled only by the dissipated power of the bias point. Fig. 1 superposes three sets of I(V) curves performed on a 4×100µm MESFET device, with different bias points corresponding to the same dissipated power of 360 mW : $V_{ds0}\times I_{ds0}$ (V×mA) = 4×90, 6×60, 12×30. Thus, the device temperature is identical for these three characterizations. The large differences between these measured I(V) characteristics are only due to the presence of trapping effects that depend on the quiescent bias point (V_{ds0}, I_{ds0}). In order to study this dependence, we have performed extensive isothermal measurements of MESFET devices, showing that hot FET trapping effects encountered in pulsed I(V) characteristics mainly depend on the V_{ds0} bias voltage. Note that the transistor was completely light-tight during measurements, because the trapping emission phenomenon is modified by light.

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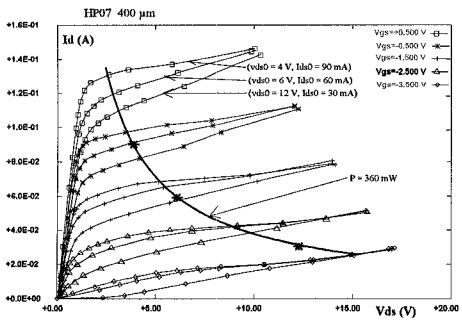

Fig. 1 : Three I(V) pulsed characteristics of a 4×100µm MESFET, for three bias points : 4 V × 90 mA, 6 V × 60 mA, 12 V × 30 mA ; 360 mW DC.

B - Drain current transient measurements

With a DC bias point and a pulsed point placed on the same dissipated power hyperbola (i.e. at the same temperature), we observe on Fig. 2 the current transients on the oscilloscope, as a result of the trapping phenomena. A constant power of 37 mW is dissipated, with V_{ds} varying from 1 V to 8.5 V. Note that this dissipated power is accurately set constant in the complete measurement cycle of Fig. 2, with a pulsed drain generator impedance adapted for that purpose.

When the drain voltage is high, electrons are captured in ionized deep level traps if the applied pulse duration is longer than the capture time constant. The capture rate has been shown to depend on the electron concentration [6], a large part of deep level traps are filled in a few tens of nanoseconds. Consequently, the space charge at the edge of the channel/substrate junction increases. This leads to the channel thickness reduction and therefore the drain current decreases to its steady state, following the filling of traps.

When V_{ds} falls from 8.5 V to 1 V, the captured electrons are slowly emitted in a few milliseconds by the deep level traps, thus the backgate potential decreases slowly. As a consequence, the channel thickness increases slowly and the drain current reaches its steady state value after 4 ms.

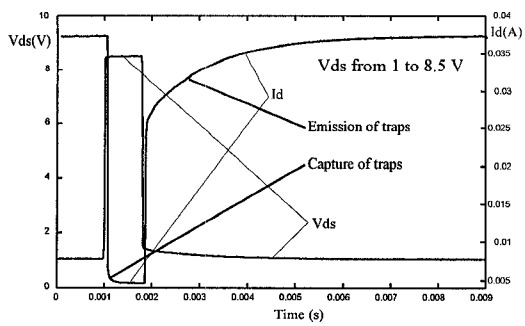

Fig. 2 : Voltage and current transients for a pulse applied along the isothermal hyperbola from V_{ds}=1V to 8.5V.

III - MEASUREMENT-BASED MODELING OF DYNAMICAL TRAPPING EFFECTS

According to the measurement results in §II-A, it is considered that the trapping effects are driven by the drain voltage. It has been shown that trapping effects can be modeled as a self backgating effect : the trapping charges are supposed to act as a pseudo-backgate terminal voltage V_B [7]. Fig. 3 represents the model topology, with the backgate potential V_B in (a) area.

The corresponding charges are stored in two capacitors C_{BD} and C_{BS} : the drain to substrate capacitor and the source to substrate capacitor respectively. The complete backgate equivalent capacitor C_B follows :

$$C_B = C_{BD} + C_{BS}$$

For DC values of the V_{DS} voltage, or in the case of low frequencies with periods much smaller than trap time constants, the capture or emission processes of electrons are completed. In that case, V_B varies proportionally with V_{DS}. This proportionality can be expressed with coefficient α_R and modeled with two serial substrate resistors connected between drain and source terminals :

$$\alpha_R = \frac{R_{BS}}{R_{BD} + R_{BS}}$$

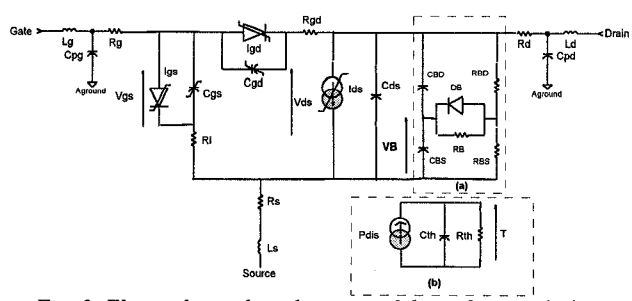

Fig. 3. Electrothermal nonlinear model topology including trapping and thermal effects

When RF signals are applied, capture or emission of traps do not have enough time to occur during the RF cycle. The backgate voltage V_B varies with the instantaneous C_{BD} charge, with a small coefficient α_C :

$$\alpha_C = \frac{C_{BD}}{C_B}$$

For intermediate frequencies, as shown in Fig. 2, V_B reaches a steady state value after a delay that depends on the sign and amplitude of the V_{DS} variation. We describe the electron capture and emission with a parallel circuit consisting of a diode, D_{BE} and a resistor, R_{BE}. The R_B resistor empties the charges in the case of emission, and capture is performed through the D_B diode. The time constants obtained with transient pulse measurements determine R_B and D_B parameters, as soon as C_{BD}, C_{BS}, R_{BS} and R_{BD} parameters are fixed. The D_B diode current is :

$$I_{dB} = I_s \times \left[\exp\left(\frac{q}{KT} \Delta V_B\right) - 1 \right]$$

When the backgate potential varies, the free electron concentration is modified leading to the change of the trap capture time constant which is expressed as :

$$\tau_C = C_B \times R_{dy} \quad \text{with} \quad R_{dy} = \frac{KT}{qI_{dB}}$$

in which R_{dy} is the diode dynamical resistor. The emission time constant, which is supposed fixed, is expressed as :

$$\tau_E = C_B \times R_B$$

The determination of C_{BD}, C_{BS}, R_{BS} and R_{BD} is based on pulsed I(V) measurements, that provide α_R and α_C parameters and on two choices : first, we want to avoid any direct electrical effect of the trap circuit in the drain output impedance. Thus, we choose very large values for these parameters. Secondly, in order to control the time constants only with R_B, D_B and C_B, the RF impedance presented by C_B must be much larger than $R_{BS} + R_{BD}$.

The α_B, α_R and α_C values are extracted from isothermal pulsed I(V) measurements for different quiescent bias points (Fig. 1). In the case of pulsed measurements with 300 ns pulse duration, capture of traps can occur during the pulses for pulse levels larger than V_{DS0}. If the pulse level V_{DSi} is smaller than V_{DS0}, pulses are too short to allow the emission phenomenon to begin. Thus, the backgate potential is calculated with the following formula in order to fit the pulsed measured I(V) curves.

$$V_B = \alpha_R \times V_{ds0} + \text{if } V_{dsi} > V_{ds0} \text{ then } \alpha_C \times (V_{ds0} - V_{dsi}) \text{ else } 0$$

The drain current generator, Ids, is controlled by two voltages, V_{gs} and V_{ds}, and is described with a Tajima model. The key point of our approach for trap phenomena modeling is to modify the V_{gs} control voltage by including the backgate voltage as follows :

$$V_{gs\_B} = V_{gs} - \alpha_B \times V_B$$

With these formulas of V_B and $V_{gs\text{-}B}$, the three static parameters α_B, α_C and α_R are simultaneously optimized with the drain current model parameters. Note that this method which takes into account trapping effects on the drain current can be implemented in various drain current models.

IV - ELECTROTHERMAL NONLINEAR MODEL

The temperature behavior of devices is measured with the pulsed set-up. The key point consists in separating trapping and thermal effects with thermal measurements performed at constant v_{ds} voltages and with the device put in a thermal enclosure.

In order to measure the device temperature, we use the embedded thermometer of the gate to source junction [8]. With a calibration of this thermometer, we obtain the temperature of the device versus its dissipated power, this leads to the thermal resistance R_{TH} [9]. The dynamical thermal effects are taken into account with a time constant provided by the foundry, they are modeled with the thermal capacitance C_{TH}.

The temperature is a command of the device. Nonlinear RF models are extracted with usual methods for several temperatures. Only a few numbers of the model parameters have exhibited a dependence with the temperature, with linear or exponential variations :

$$I_{dss} = I_{dsst} \times \exp\left(-T/T_{ds}\right) + I_{dss0} \quad \text{(Tajima model)}$$

$$P = P_t \times T + P_0 \quad \text{(Tajima model)}$$

$$I_{s\_gs} = I_{sgst} \times \exp\left(-T/T_{sgs}\right) + I_{sgs0} \quad \text{(Gate / Source diode)}$$

$$N_{gs} = N_{gst} \times T + N_{gs0} \quad \text{(Gate / Source diode)}$$

$$I_{s\_gd} = I_{sgdt} \times \exp\left(-T/T_{sgd}\right) + I_{sgd0} \quad \text{(Gate / Drain diode)}$$

$$N_{gd} = N_{gdt} \times T + N_{gd0} \quad \text{(Gate / Drain diode)}$$

With a virtual temperature circuit (R_{TH}, C_{TH} and P_{dis} area (b) on Fig. 3), harmonic balance simulators can compute the device temperature and feed back to the model [9].

V - RESULTS

The trapping effects and thermal effects have been implemented in the same MESFET model in a commercially available microwave simulator. This model also includes nonlinear gate capacitances derived from pulsed RF measurements [2].

To test the validity of our model under pulsed measurement conditions, we simulate the pulsed measurement set-up with a time domain simulator (SPICE), as shown in Fig. 4. Starting from the quiescent bias point (V_{gs0}, V_{ds0}), pulses are applied to describe the device dynamical behavior.

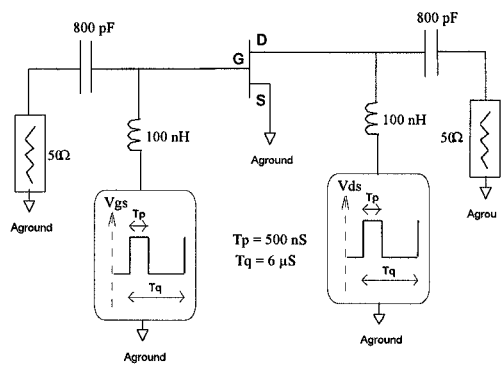

Fig. 4. Simulated pulsed measurements set-up

We can vary the pulsed voltages, (V_{gsi}, V_{dsi}) so as to generate a set of I(V) pulsed curves. Fig. 5 shows simulated pulsed I(V) characteristics compared with measurement ones for two quiescent bias points (V_{ds0} = 4, 12 V ; I_{ds0} = 90, 30 mA). The pulse duration and periods are identical. We note a good agreement between measurement and model results performed for a large variation of V_{ds0}.

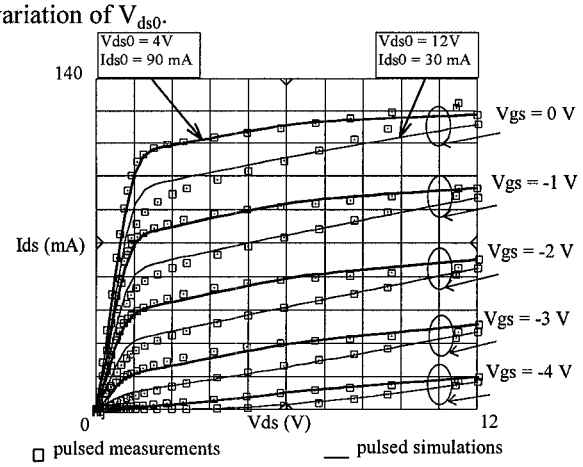

Fig. 5 : pulsed I(V) measurement and model for two bias points.

Trapping effects induce a dispersive output impedance of devices at low frequencies. Fig. 6 shows the output impedance simulated from the proposed nonlinear model. Measurements performed with a low frequency analyser (HP 4194) have confirmed the LF and HF values of the output impedance. A transition frequency of 3 KHz was measured for the same bias point as well as an output impedance of 300 Ω.

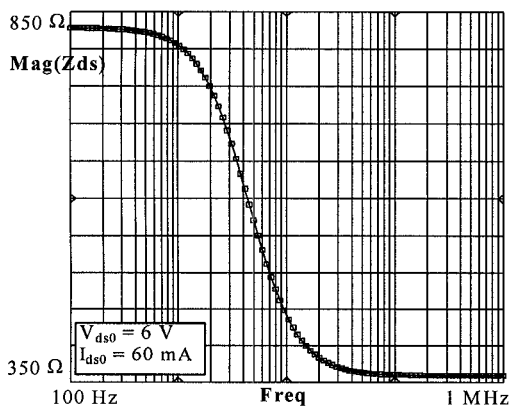

Fig. 6 : Frequency dispersion of the MESFET model output impedance.

10 Ghz load-pull measurements have been carried out for several biasing conditions. Fig. 7 presents measured and simulated output power and efficiency for the quiescent bias point V_{ds0} = 12 V, I_{ds0} = 30 mA. We can notice that the error on output power is smaller than 0.5 dB ; the efficiency is computed with an accuracy better than 1.5 %. The same quality of simulation is achieved for the other bias points (A class, AB class, B class).

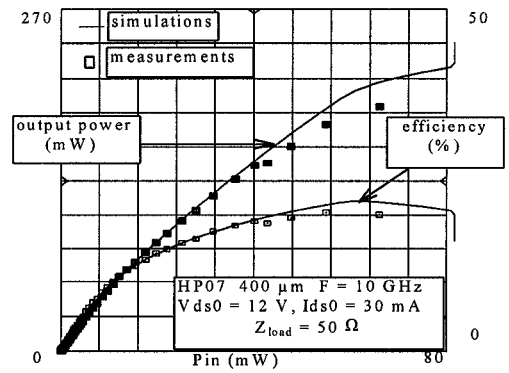

Fig 7 : Measured and simulated output power and efficiency

CONCLUSION

We have developed a nonlinear dynamic model of MESFETs that includes trapping and thermal phenomena. This large-purpose model is derived from pulsed I(V) and pulsed RF measurements, it is suitable for standard microwave C.A.D. softwares. The handle of thermal and trapping effects makes our nonlinear model versatile and accurate for all hot FET biasing conditions. The dispersive effect of traps is computed, as well as the thermal time constant, providing the capability to take into account slow dynamics. This model, accurate from DC to microwave frequencies, offers new perspectives of reliability and flexibility for MMIC circuit design.

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